1. Cache Indexing:

Mapping	Address Space Size	Cache Size	Block Size	Tag Field	Index Field	Offset Field
Direct	1MB	8KB	4B			
Fully Assoc.						
2-Way						
Direct	1MB	16KB	8B			
Fully Assoc.						
4-Way						
Direct	1MB	32KB	8B			
Fully Assoc.						
2-Way						
Direct	4GB	128KB	16B			
Fully Assoc.						
4-Way						
Direct	4GB	512KB	16B			
Fully Assoc.						
4-Way						

2. Explain the difference between a direct-mapped , set associative and fully associate cache organizations showing different fields in their memory address.

3. Consider a processor with 32 byte memory (i.e., 5 bit address) and 8 byte direct-mapped cache. Assume the cache block size is 1 byte. Table below shows the current state of the cache. For each of the memory reference in the reference sequence 10011, 00001, 00110, 01010, 01110, 11001, 00001, and 11100, identify whether the reference is a cache hit or miss. If it is a miss, identify the type of the miss (i.e., compulsory, conflict, or capacity). Answer by filling out the Table 2.

Index	V	Tag	Data
000	N		
001	Y	00	Mem(00001)
010	N		
011	Y	11	Mem(11011)
100	Y	10	Mem(10100)
101	Y	01	Mem(01101)
110	Y	00	Mem(00110)
111	N		

Table 1

Reference	H/M	Type
10011		
00001		
00110		
01010		
01110		
11001		
00001		
11100		

Table 2

4. How is a virtual address translated to physical address by the operating system?

If a system has 32-bit virtual address, 4-KB pages and 32-bit physical address, how much memory is consumed for keeping page tables for 100 processes?

How can the memory space overhead be reduced?

How can memory access overhead be reduced?

5. What is the maximum memory capacity supported by the following server: 2 processor sockets, each socket has 4 memory channels, each channel supports 2 dual-ranked DIMMs, and x4 4Gb DRAM chips? Assume 64-bit data bus

6. PAGE TABLES. Consider the following parameters.
   Page size: 16KBytes
   Page table: four-level page table.
   The virtual page number is split in 4 fields of 9 bits each.
   Entries in all tables are 32 bits (4 bytes).
      a. Which bits of the virtual address are used to index the first level table (top level in the hierarchy):

      b. Which bits of the virtual address are used to index the page tables at the bottom of the hierarchy:

      c. What is the size of each table at all levels (in bytes)?

      d. What is the total amount of virtual memory covered by one entry of page tables at each level:

7. TLB. Continuing from the previous problem, consider the following parameters.
   TLB size: 128 entries
   TLB organization: 4-way set-associative
      a. Which bits of the virtual address are used to index the TLB:

      b. Which bits of the virtual address are used as tags in the TLB?

      c. TLB tag size:

Other conceptual questions can include:
Thread-level parallelism
Data-level parallelism
Main memory
Cache
GPGPUs
Datacenters